A 15GHz SINGLE STAGE GaAs DUAL-GATE FET MONOLITHIC ANALOG FREQUENCY DIVIDER WITH REDUCED INPUT THRESHOLD POWER

Kunihiko Kanazawa, Masaru Kazumura, and Gota Kano

Matsushita Electronics Corporation
Electronics Research Laboratory
1-1 Saiwaicho, Takatsuki, Osaka, Japan

ABSTRACT

A 15GHz single stage GaAs dual-gate FET monolithic analog frequency divider with the reduced input threshold power has been designed and fabricated. Use of the dual-gate structure for the FET mixer contributed to simplifying the circuit configuration. Introduction of the rejection filter at the output port resulted in reducing the input threshold power down to 1.4dBm.

INTRODUCTION

An analog frequency divider [1], which operates on the base of induced subharmonic oscillation, is receiving growing interests in the field of microwave communication systems [2]-[5]. Fig.1 shows a diagram of the regenerative analog frequency divider being composed of a mixer, a bandpass filter, amplifiers, and a feedback circuit. Although this analog frequency divider is inherently suitable for the high frequency operation, it possesses following two substantial drawbacks. One is that the complex circuit configuration is needed because of poor separation of the signals [1],[4]. The other is that the input threshold power is undesirably high [4]-[5].

The purpose of the present study is to improve these drawbacks by using the dual-gate structure for the FET mixer so as to improve the isolation of the signals and by introducing the rejection filter at the output port so as to increase the conversion gain. The dual-gate FET contributes to simplifying the circuit configuration. The rejection filter results in reducing the input threshold power. This paper describes a work undertaken to design, fabricate and test the 15GHz single stage GaAs dual-gate FET monolithic analog frequency divider with the reduced input threshold power.

DESIGN

For the purpose of achieving the simple circuit configuration, the dual-gate FET being suitable for avoiding cumbersome passive couplers is utilized as the mixing element. This dual-gate FET mixer is designed to have so high gain that the amplifiers in the loop in Fig.1 can be removed.

An equivalent circuit of the single stage dual-gate FET analog 1/2 frequency divider is shown in Fig.2. Techniques used for reducing the input threshold power are as follows.

1) suppression of the input frequency Fin signal at the drain port of the dual-gate FET.
2) minimization of the loss of the input matching circuit.
3) optimization of the geometric parameters of the dual-gate FET.
4) suppression of the loss of the 1/2 Fin signal in the loop.

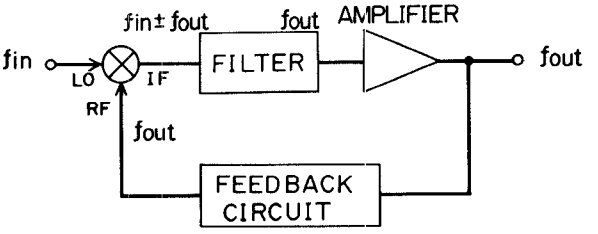

Fig. 1. Block diagram of the regenerative analog frequency divider.

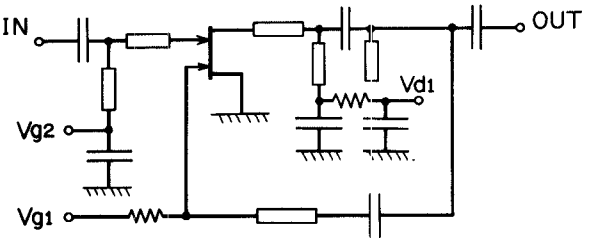

Fig. 2. Equivalent circuit of the single stage dual-gate FET analog 1/2 frequency divider.

CH2591-6/88/0000-0047$01.00 © 1988 IEEE

The attention was focused on the suppression of the Fin signal at the output port of the dual-gate FET by using the rejection filter. This results in the reduction of the input threshold power because the suppression of the Fin signal contributes to increasing the conversion gain of the dual-gate FET mixer by returning the LO signal to the mixer output port [7]. It is noted that a very compact spiral open stub is used as the rejection filter. The techniques 2), 3), and 4) are achieved as follows. The minimization of the input matching loss was performed by the computer simulation of the matching circuit composed of two microstrip lines. The optimization of the FET parameters were also carried out by the computer simulation. The optimized FET parameters are the gate length / width as 0.7μm / 300μm. The suppression of the loop loss for the 1/2 Fin signal was realized by optimizing the length of the feedback microstrip line to be 10.6mm.

FABRICATION

The process used was the full ion-implantaion process, LATIT (Local Area Through-oxide Implantation Technology) [6]. The n-type active and n^+-type contact layers were provided by selective ion implantaion of Si onto an undoped LEC GaAs substrate under the condition of 1×10^{13} cm^{-2} dose at 70 keV and 5×10^{13} cm^{-2} dose at 140 keV, respectively. Au/Ni/AuGe and Al/Ti were used for the Ohmic contacts and the Schottky gate, respectively.

The photograph of the chip of the analog frequency divider with an IF buffer amplifier is shown in Fig. 3. The chip size measures 1.2 x 1.4mm.

TEST RESULTS

The input threshold power is measured as a function of the input frequency as shown in Fig. 4. No additional matching circuit is used for 50-Ω measurement set-up. The minimum input threhold power is as low as 1.4dBm at a input frequency of 14.7GHz. The operation frequency band ranges from 14.2GHz to 15.3GHz. The input and output waveforms observed are shown in Fig. 5. This well-shaped output waveform is due to the fact that the signal of the input frequency Fin is efficiently suppressed at the output port. The measured input/output characteristics at 14.8GHz are shown in Fig. 6. The high conversion gain of 0.0-2.5dB is obtained for the input power of 2.0-9.5dBm.

CONCLUSION

It is shown that the 15GHz single stage GaAs dual-gate FET monolithic analog frequency divider with the reduced input thresold power has been designed and fabricated. Use of the dual-gate FET

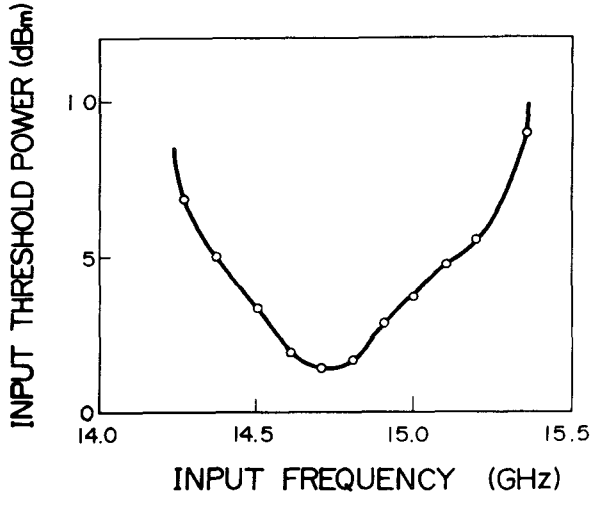

Fig. 4. Measured input threshold power as a function of the input frequency.

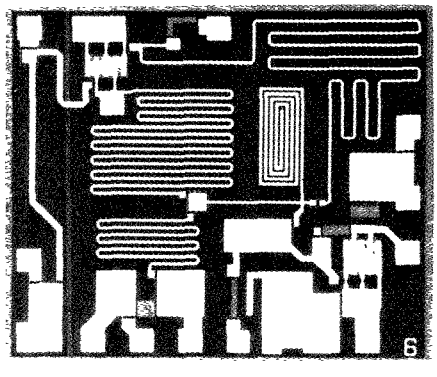

Fig. 3. Photograph of the 15GHz single stage GaAs dual-gate FET monolithic analog frequency divider with an IF amplifier.

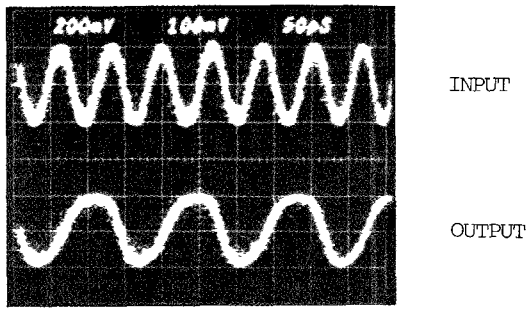

Fig. 5. Measured input and output waveforms at the input frequency of 14.8GHz.

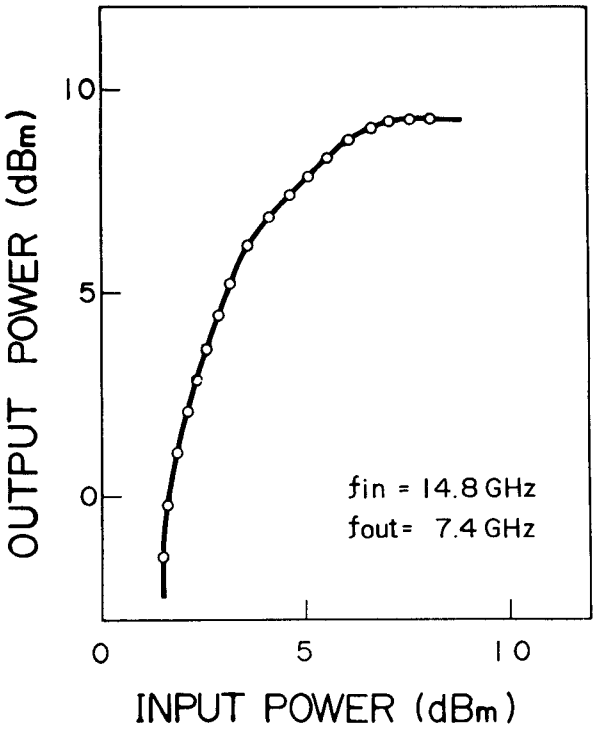

Fig. 6. Measured input/output characteristics at the input frequency of 14.8GHz.

and introduction of the rejection filter contributed to simplifying the circuit configuration and reducing the input threshold power, respectively. This analog frequency divider MMIC exhibited the 1.4dBm input threshold power.

ACKNOWLEDGMENT

The authors wish to thank M. Hagio and Dr. I. Teramoto for their constant encouragement throughout this study.

REFERENCES

[1] R.L.Miller,"Fractional-frequency generators utilizing regenerative modulation,"Proc. IRE, vol.27, pp.446-456, July, 1939.
[2] C.Rauscher,"Regenerative frequency division with a GaAs FET",IEEE Trans. Microwave Theory Tech. vol.MTT-32, pp.1461-1468.
[3] D.Kaminsky,P.Goussu,R.Funck, and A.G.Bert,"A dual-gate GaAs F.E.T. analog frequency divider",IEEE MTT-S digest, 1983.
[4] T.Ohira,K.Araki,T.Tanaka,and H.Kato,"14GHz band GaAs monolithic analog frequency divider", Electronics Letters,vol.21,pp.1057-1058, Oct.1985.
[5] K.Honjo and M.Madihian,"Novel design approach for X-band GaAs monolithic analog 1/4 frequency divider", IEEE Trans. Micrwave Theory Tech. vol.MTT-34, pp.436-441, April,1986.
[6] M.G.Stubbs and S.P.Stapleton, "A single stage monolithic regenerative 1/2 analog frequency divider", IEEE GaAs IC Symposium digest, pp.199-201, 1986.
[7] P. Harrop,"Gallium arsenide field transistor mixers : theory and applications", ACTA Electonica, vol. 23, pp. 291-297, April, 1980.